(Pages : 3) **6558**

Reg. No. : .....

Name : .....

# Third Semester B.Tech. Degree Examination, November 2014
## (2013 Scheme)
## 13.305 : DIGITAL SYSTEM DESIGN (FR)

Time : 3 Hours Max. Marks : 100



### PART – A

Answer for **all** questions. **Each** question carries **2** marks.

1. Realize a XOR gate with NAND only circuit.
2. Write the canonical SOP expression for the given function.
   $f(x_1, x_2, x_3) = \Sigma\, m\,(2, 3, 4, 6, 7)$
3. Draw a neat block diagram for a Serial In Parallel Out shift register.
4. Give the truth table and logic diagram for T Flip Flop.
5. What is the role of a state diagram in simplification of a sequential circuit ?
6. List the limitations of asynchronous counter.
7. Give the syntax for 'signal' declaration statement in HDL.
8. Give the schematic diagram for Random Access Memory (RAM).
9. Perform $0.101 \times 2^3 + 0.111 \times 2^5 = ?$
10. Draw the logic diagram of a 4 bit by 3 bit array multiplier. **(10×2=20 Marks)**

### PART – B

Answer **any one** question from **each** Module. **Each full** question carries **20** marks.

**Module – I**

11. a) Design a full adder circuit and draw the logic diagram using gates. **10**

    b) Using a four variable K map, simplify the given expression.
    $f = \Sigma m\,(1, 2, 4, 6, 10, 11, 13, 15)$. **10**

OR

P.T.O.

12. a) Reduce the expression $S = \sum m(1, 2, 4, 6, 9, 11, 15) + d(3, 10, 14)$ by using a four variable K-map method. **14**

b) State and prove DeMorgan's theorem. **6**

## Module – II

13. a) What is multiplexer ? Derive a logic diagram for a 8 : 1 multiplexer. **8**

b) Design a sequential circuit whose state table is given below. Draw the state diagram and realize the circuit using JK FF. **12**

| Present State | Next State | | Output | |
|---|---|---|---|---|
| | X = 0 | X = 1 | X = 0 | X = 1 |
| 001 | 001 | 010 | 0 | 0 |
| 010 | 001 | 100 | 0 | 0 |
| 100 | 101 | 100 | 0 | 1 |
| 101 | 001 | 100 | 0 | 1 |

OR

14. a) Reduce the given state table for minimum state, then find the output sequence generated with an input sequence of '0111001001'. Start from the state 'A'. **12**

| Present State | Next State | | Output | |
|---|---|---|---|---|
| | X = 0 | X = 1 | X = 0 | X = 1 |
| A | A | E | 0 | 0 |
| B | C | B | 0 | 1 |
| C | A | F | 0 | 0 |
| D | C | B | 0 | 1 |
| E | F | E | 0 | 0 |
| F | A | F | 0 | 0 |
| G | F | G | 0 | 1 |

b) What is a decoder ? Derive a logic diagram for a 4 to 10 line decoder. **8**

## Module – III

15. a) Draw the circuit diagram for a 3 bit Johnson Counter and show how the data gets shifted in each clock. 10

    b) Differentiate PAL and PLA with the help of a neat structural diagram. 10

OR

16. a) Draw the logic circuit of a mod-6 synchronous up-down counter with JK FF and explain the operation with the help of a timing diagram. 10

    b) Write a HDL code for realizing 4 : 1 Multiplexer, use behavioral model. 10

## Module – IV

17. a) Explain the implementation of a Combinational Multiplication for $8 \times 8$ multiplier. 15

    b) Give the state graph for a binary addition control network. 5

OR

18. a) Perform the 3 bit by 2 bit signed division using shift and subtract algorithm. 10

    b) Explain the Booth's algorithm for performing multiplication of $8 \times 8$ multiplier. 10

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